Printed pages: 02 **Sub Code: NCS 505**

PaperID | 1 | 0 | 4 | 0 | **Roll** | | | | | | | | | | **No.**

B.TECH
(SEM V) THEORY EXAMINATION 2017-18
COMPUTER ARCHITECTURE

Time: 3 Hours ***Total Marks: 100***

Note: 1. Attempt all Sections. If any missing data is required, then choose suitably.

SECTION A

1. Attempt *all* questions in brief. **2 x10 = 20**

a. What is meant by synchronous and asynchronous communication?
b. Describe magnetic disk?
c. What is instruction cycle?
d. Discuss floating point number representation.
e. Explain concept of memory transfer.
f. What are various types of registers?
g. Define bus arbitration. What the different types are of bus arbitration do you know?
h. What is auxiliary memory? Explain.
i. What is vertical microprogramming?
j. How may 128X8RAM chips are needed to provide memory capacity of 2048 bytes?

SECTION B

2. Attempt any *three* of the following: **10 x 3 = 30**

a. Explain General Register Organization with the help of suitable diagram.
b. What is interrupt? What are the different types of interrupts?
c. Describe the following organizations of cache memory:
   (i). Associative mapping
   (ii). Direct Mapping
   (iii). Set associative mapping
d. A digital computer has a memory unit of 64K X 16 and a cache memory of 1K words. The cache uses direct mapping with block size of four words.
   (i). How many bits are there in tag, index, block and word fiels of the address format?
   (ii). How many bits are there in each word of cache, and how they are devided into functions? Include a valid bit.
   (iii). How many blocks can the cache accommodate?
e. Discuss stack organization. Explain the following in details.
   (i) Register stack
   (ii) Memory stack

https://quescol.com | Free PYQs, Solutions, Syllabus, Notes etc

SECTION C

3. Attempt any *one* part of the following: 10 x 1 = 10

(a) Discuss Booth's algorithm. Multiply (-7) and (3) using Booth's algorithm.

(b) Consider a two level memory hierarchy of the form (M_1, M_2) where M_1 is connected directly to the CPU. Determine the average cost per bit C and average access time t_a for the data given below:

Level(i)	Capacity(S_i)	Cost(C_i)	Access time (t_{ai})	Hit Ratio(H)
M_1 (Cache)	1024	0.1000	10^{-8}	.9000
M_2 (Main)	2^{16}	0.0100	10^{-6}	-

4. Attempt any *one* part of the following: 10 x 1 = 10

(a) Discuss control word with suitable example.

(b) Describe I/O interface.

5. Attempt any *one* part of the following: 10 x 1 = 10

(a) What is DMA in computer architecture?

(b) Draw and explain **2D** and **2-1/2D** RAM chip

6. Attempt any *one* part of the following: 10 x 1 = 10

(a) What is Virtual Memory? Why is it necessary to implement virtual memory? What is use of page replacement algorithm?

(b) What is difference between I/O mapped input/output and memory mapped I/O? What are the advantages and disadvantages of each?

7. Attempt any *one* part of the following: 10 x 1 = 10

(a) Write a program to evaluate arithmetic expression
X= (A – B) * (((C -D) / F) / G)
Using a general register computer with three, two, one & zero address instructions.

(b) Describe the following control units
(i). Hardwired control unit
(ii).Microprammed control unit

quescol.com