(Following Paper ID and Roll No. to be filled in your Answer Book)

PAPER ID : 110401

Roll No.

B. Tech.

(SEM. IV) THEORY EXAMINATION, 2014-15

COMPUTER ORGANIZATION

Time : 3 Hours] [Total Marks : 100

Note:(1) Attempt all questions.

(2) Make suitable assumptions wherever necessary.

Attempt any **two** parts of the following: [10×2=20]

(a) What is a multiplexer and demultiplexer ? Explain how an 8 x 1 multiplexer can designed using two 4x1 multiplexers.

(b) (i) Simplify the following function using k map and draw the circuit using AND, OR, NOT gates.

F(A, B, C, D) = s(0, 2, 8, 9, 10, 11, 13, 15)

(ii) Add – 35 and -31 in binary using 8 bit registers, in signed 1's complement and signed 2's complement

(c) Show step by step the multiplication process using booth's algorithm when (+15) and (-13) numbers are multiplied. Assume 5-bit registers that hold signed numbers.

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Attempt any **two** parts of the following : [10×2=20]

(a) What is an instruction in the context of computer organization ? Explain the purpose of various elements of an instruction with the help of a sample instruction format.

(b) Explain the following addressing modes with the help of an example each:

(i) Direct

(ii) Register Indirect

(iii) Implied

(iv) Immediate

(v) Indexed

(c) Write the steps in fetching a word from memory. Differentiate between a branch instruction and call subroutine instruction.

Attempt any **two** parts of the following : [10×2=20]

(a) Compare and contrast hardwired and micro programmed control units. Also lists their advantages and disadvantages.

(b) What are the different categories of micro-operations that may be carried out by CPU? Explain each category of micro-operations giving one example for each.

(c) Write short notes on the following:

(i) Micro program sequencer for control memory.

(ii) RISC.

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Attempt any **two** parts of the following: [10×2=20]

(a) What is the difference between isolated I/O and memory mapped I/O? Explain the advantages and disadvantages of each.

(b) Consider a cache uses a direct mapping scheme. The size of main memory is 4K bytes and word size of cache is 2 bytes. The size of cache memory is 128 bytes. Find the following:

(i) The size of main memory address (assume each byte of main memory has an address)

(ii) Address of cache block

(iii) How many memory location address will be translated to cache address/block/location?

(iv) How can it be determined if the content of specified main memory address exists in cache.

(c) Explain the following memory schemes discussing why needed the :

(i) Interleaved memory

(ii) Associative memory

Write short notes on any **four** of the following: [5×4=20)

(a) Interrupt

(b) Bus arbitration

(c) Virtual Memory

(d) Organization of 2D and 2 ½ D.

(e) Programmed I/O

(f) DMA.

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