(Following Paper ID and Roll No. to be filled in your Answer Book)

PAPER ID : 0109 **Roll No.** | | | | | | | | | | |

B.Tech.

(SEM. III) ODD SEMESTER THEORY EXAMINATION 2012-13

DIGITAL LOGIC DESIGN

Time : 3 Hours *Total Marks : 100*

Note :—*(1) Attempt **all** questions.*

(2) All questions carry equal marks.

1. Attempt any **TWO** parts of the following : **(10×2=20)**

(a) (i) What do you mean by sign magnitude representation ? Discuss.

(ii) Explain the rules of 2's complement addition and subtraction with suitable examples.

(b) (i) Simplify the following Boolean equation :

$$Y(A, B, C, D) = \overline{A}\ \overline{B}\ C\ \overline{D} + \overline{A}\ \overline{B}\ \overline{C}\ \overline{D}$$

(ii) Minimize the following logic function using K-map :

$$Y(A, B, C, D) = \Sigma\ m(0, 1, 2, 3, 4, 7, 8, 9, 10, 11, 12, 14)$$

and implement it using logic gates.

(c) What is BCD code ? What are the rules for BCD addition ? Explain with suitable example.

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2. Attempt any **TWO** parts of the following : **(10×2=20)**

(a) (i) Design a combinational logic circuit with three input variables that will produce logic 1 output when more than one input variables are logic 0.

(ii) Draw logic diagram of half subtractor.

(b) Draw and explain the carry look ahead adder.

(c) Implement the following function using a 4 : 1 multiplexer :

$f(A, B, C, D) = \Sigma\, m(2, 3, 5, 7, 8, 9, 12, 13, 14, 15)$.

3. Attempt any **TWO** parts of the following : **(10×2=20)**

(a) Explain J-K flip flop with preset and clear. Also draw the logic circuit of SR flip flop using T flip flop.

(b) Design a divide by 7 counter with suitable diagram.

(c) Design a 4 bit binary up down ripple counter. Also show its clock diagram.

4. Attempt any **TWO** parts of the following : **(10×2=20)**

(a) Explain PLA with the help of block diagram.

(b) (i) Write short on EPROM.

(ii) Differentiate static RAM and dynamic RAM.

(c) Implement the following Boolean expressions using PROM :

(i) $F1\ (A, B, C) = \Sigma m(0, 2, 4, 7)$

(ii) $F2\ (A, B, C) = \Sigma m(1, 3, 5, 7)$

5. Attempt any **TWO** parts of the following : **(10×2=20)**

(a) Design an asynchronous sequential circuit with two input, I_1 and I_2 and one output Z. Initially, both inputs

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are equal to zero. When I_1 or I_2 becomes 1, Z becomes 1. When the second input goes to 1, the output changes from 1 to 0. The output stays at 0 until the circuit goes back to (0, 0).

(b) Draw an ASM chart for a modulo-4 UP/DOWN counter having the state transition table as given below :

Present State	Next State	
	X = 0	X = 1
0 0	0 1	1 1
0 1	1 0	0 0
1 0	1 1	0 1
1 1	0 0	1 0

(c) What is the significance of state assignment ? List the different techniques used for state assignment and discuss any one of them.

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